

Suspended graphene devices with local gate control on an insulating substrate

Florian R Ong^{1‡}, Zheng Cui¹, Muhammet A Yurtalan², Cameron Vojvodin¹, Michał Papaj¹, Jean-Luc F X Orgiazzi², Chunqing Deng¹, Mustafa Bal^{1§} and Adrian Lupascu¹

¹ Institute for Quantum Computing, Department of Physics and Astronomy, and Waterloo Institute for Nanotechnology, University of Waterloo, Waterloo, Ontario N2L 3G1, Canada

² Institute for Quantum Computing, Department of Electrical Engineering, and Waterloo Institute for Nanotechnology, University of Waterloo, Waterloo, Ontario N2L 3G1, Canada

E-mail: florian.ong@uibk.ac.at, alupascu@uwaterloo.ca

Abstract. We present a fabrication process for graphene-based devices where a graphene monolayer is suspended above a local metallic gate placed in a trench. As an example we detail the fabrication steps of a graphene field-effect transistor. The devices are built on a bare high-resistivity silicon substrate. At temperatures of 77 K and below, we observe the field-effect modulation of the graphene resistivity by a voltage applied to the gate. This fabrication approach enables new experiments involving graphene-based superconducting qubits and nano-electromechanical resonators. The method is applicable to other two-dimensional materials.

Keywords: suspended graphene, field-effect transistors, 2D materials

Submitted to: *Nanotechnology*

‡ Present address: Universität Innsbruck, Institut für Experimentalphysik, Technikerstrasse 25/4, A-6020 Innsbruck Austria

§ Present address: TUBITAK Marmara Research Centre, Materials Institute, P.O. Box 21, 41470 Gebze, Kocaeli, Turkey

1. Introduction

Graphene physics has become a broad and very active field of research since single-layer graphene sheets have been successfully isolated ten years ago [1]. On the one hand, exceptional structural properties, such as two-dimensional crystalline order over macroscopic scale, make graphene a rich playground for investigating fundamental physics problems. Graphene research topics include dynamics of massless Dirac fermions [2], quantum Hall effect [3], Klein paradox [4], conductance quantization [5], quantum billiards [6], and superconducting proximity effect [7]. On the other hand, the potential applications of graphene in micro- and nanotechnologies have triggered intense interest [8, 9]. For instance, the outstanding electrical and mechanical properties of graphene could be the basis for next-generation transistors [10, 11] and for classical and quantum nano-electromechanical (NEM) devices [12, 13]. Graphene is a versatile material allowing 2D electronic transport to be investigated in different regimes. By patterning devices with a length of the conduction channel varying by orders of magnitude (a few tens of nanometers up to centimeters), one easily explores the ballistic and diffusive regimes of electronic transport. Moreover, applying an electric field in the vicinity of a graphene sheet allows to change the nature of the charge carriers (electrons or holes) and to modulate their surface density. This offers a new degree of freedom compared to metals or 2D electron gases in GaAs/GaAlAs heterostructures.

A convenient method to study electron transport in graphene is based on the field effect transistor (FET) geometry, where a graphene sheet is galvanically connected to two metallic electrodes and capacitively coupled to a metallic gate [1]. The easiest and most common route of fabricating such devices relies on a doped semiconducting substrate covered by an insulating layer. The substrate, typically doped silicon, is used as a back-gate to modulate the density of carriers in graphene. Although this method and its refinements have proven very successful, in practice it has the following limitations in investigating the properties of graphene. Firstly, there is evidence that the intrinsic properties of graphene are impaired when directly lying on a bulk material (the insulating layer in this case). Interactions with the substrate introduce a scattering mechanism for electrons travelling through the conducting channel which reduces their mobility [14, 15] (a noteworthy exception is boron nitride substrate, onto which graphene performs well due to the matching of both hexagonal lattices [16]). Secondly, trapped charges in the oxide locally modify the electrical potential set by the back-gate [17]. Lastly, the use of the substrate as a back-gate makes it difficult to integrate several graphene devices on the same chip, for which multiple local gates are required.

The presence of a doped substrate is also detrimental to systems sensitive to energy losses. This includes superconducting qubits and electromagnetic resonators operating in the GHz frequency range. Superconductor-graphene-superconductor (S-G-S) junctions have been shown to exhibit Josephson tunneling with a critical current tunable by the gate voltage [7, 18, 19]. In a S-G-S junction the tunnel barrier is formed by a graphene

sheet contacted laterally by superconducting electrodes, in a configuration similar to that of long superconductor-normal metal-superconductor junctions [20]. S-G-S junctions could be used as building blocks for superconducting qubits, SQUIDs [21, 22], and superconducting circuits to study quantum optics at microwave frequencies [23]. In state-of-the-art superconducting qubits, the amorphous nature of the oxide forming the Josephson junctions sets a limit on performances: structural defects in the barriers result in fluctuating electric and magnetic fields that couple to the qubit and impair its coherence [24]. Replacing the amorphous oxide with a well-ordered material like graphene has the potential to improve the coherence times of superconducting qubits. However, qubits with long coherence times as well as microwave resonators with high quality factors are produced on insulating substrates such as high-resistivity silicon or sapphire [25, 26]. In this context, using a doped silicon substrate to gate a graphene Josephson junction must be avoided since its high density of mobile carriers leads to unacceptable radiofrequency losses. This problem may also be of concern in graphene NEMs operating in the GHz frequency range.

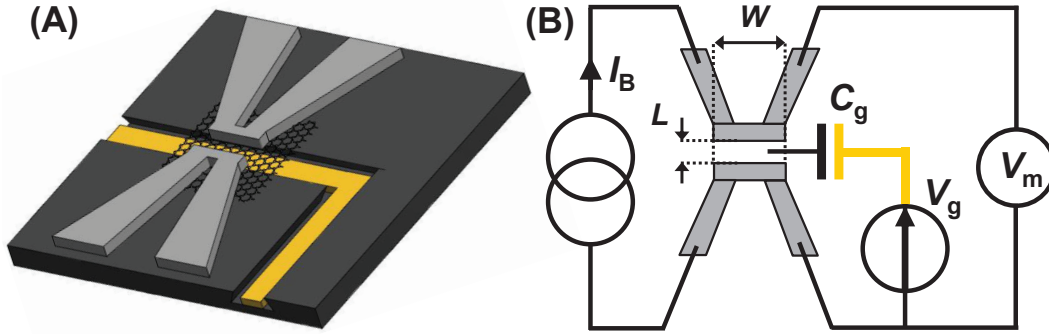


Figure 1. (color online) Overview of a suspended graphene junction. (A) Cartoon picture of the device (not to scale): a trench is etched in the silicon substrate (dark gray). A local gate (yellow) is deposited at the bottom of the trench. The graphene monolayer (honeycomb pattern) is suspended above the gate. Electrodes (gray) are evaporated to contact the graphene. (B) Sketch of the electrical setup to characterize the field-effect properties of the device, as discussed in the main text.

In this article we present a fabrication method that circumvents the aforementioned drawbacks of graphene devices fabricated on doped silicon substrate. Some of the problems have already been addressed separately. Local gates have been implemented [10, 27, 28]. FETs based on suspended graphene have been successfully fabricated, preventing interaction with the substrate and demonstrating an enhanced mobility [29]. However, to the best of our knowledge, there is no report yet of a suspended graphene FET with a local gate built on an insulating substrate. We note that two recent publications [30, 31] describe a fabrication process that shares common features with our own. However, our approach to fabrication of suspended graphene with local gating

includes a robust and well established recipe for low contact resistances. While designs in Refs. [30, 31] appear to be robust against contact resistance, other resonator designs may require lower contact resistances. Low contact resistances are essential in view of realizing S-G-S Josephson junctions [32].

A schematic picture of our suspended graphene junction is shown in figure 1(A). The substrate is unoxidized high-resistivity silicon. A trench is etched in the silicon. A metallic electrode is deposited at the bottom of this trench to be used as a gate. A graphene monolayer is suspended over the trench. The gate is separated from the graphene only by air (or vacuum). The ohmic contacts are deposited over the graphene sheet at the edge of the trench, ensuring that the whole surface of the conduction channel — called junction all along this paper — is suspended. The conductance of the device (including that of the junction and its ohmic contacts) is measured as a function of gate voltage V_g in a 4-point configuration, as shown in figure 1(B). The devices investigated in this work have a short ($L = 350 - 500$ nm) and wide ($W = 4 - 7$ μm) conduction channel, exhibiting typical graphene FET behaviour at low temperatures (4 to 77 K). The performance is comparable to that of unsuspended devices, with mobilities around $10,000$ $\text{cm}^2/\text{V/s}$ at a carrier density of $n = 10^{11}$ cm^{-2} . However, the charge degeneracy point is found to be closer to zero gate voltage than that of typical graphene FETs lying on oxide, as expected and previously demonstrated for other types of suspended devices [33].

The graphene junctions we introduce in this work satisfy all the requirements of high-transparency graphene Josephson junctions that could be used as building blocks for superconducting qubits. Indeed, compared to other recent implementations of suspended junctions [34], our device lies on an insulating substrate, an important requirement for quantum information processing based on superconducting qubits. Moreover, the junctions could yield a well-controlled environment to investigate noise properties of transport in graphene [35, 36]. Finally, the fabrication process we introduce here could be adapted to fabricate nano-electromechanical resonators where a vibrating suspended graphene bridge or membrane is actuated at high frequency by a local gate [37].

The paper is structured as follows: in Section 2 we describe the fabrication process of the device in detail. In Section 3 we present field-effect measurements carried out on a typical device at temperatures ranging from 4 K to 300 K. At room temperature, gate leakages through the imperfectly insulating substrate degrade the FET behaviour. At low temperature these leakages are suppressed and the device performs normally. We provide a model for the gate leakages, before focusing on the field-effect at low temperature. Finally we discuss experiments with other similar devices.

2. Fabrication of the suspended junctions

Suspended graphene junctions are fabricated in three main steps. Firstly, a trench is etched into the substrate and a metallic gate is deposited at the bottom of the trench. Secondly, a graphene monolayer is exfoliated, transferred and placed across the trench

and above the gate. In the last step, electrodes are patterned to electrically contact the graphene flake on both sides of the trench.

2.1. Fabrication of the local metallic gate

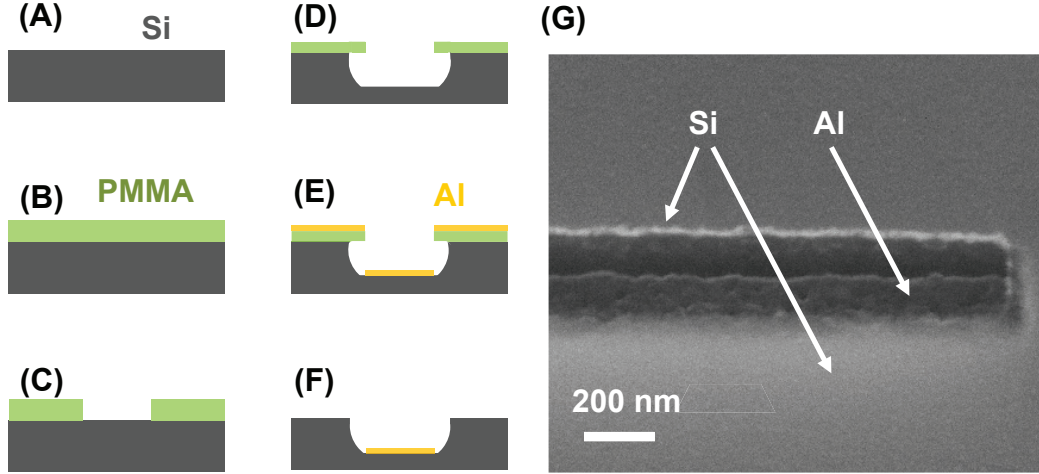


Figure 2. (color online) Fabrication of the local gate. (A) Clean bare silicon substrate. (B) Spinning of electronic beam resist (PMMA). (C) Electron beam lithography and development. (D) Dry etching of silicon. (E) Metal evaporation. (F) Lift-off. (G) Scanning electron micrograph (tilted by 45°) of a gate after lift-off.

Figure 2 describes the successive steps of fabrication of the gate. Figure 2(A): The fabrication starts with a high resistivity silicon substrate (resistivity higher than $10 \text{ k}\Omega\cdot\text{cm}$). Figure 2(B): The substrate is coated with a layer of polymethylmethacrylate (PMMA) resist. The resist will be used both as an etching mask and as a lift-off sacrificial layer. Figure 2(C): The trench profile is patterned by electron-beam lithography (EBL). Figure 2(D): Isotropic reactive ion etching is performed to etch away 230 nm of silicon. The etching process is carried out using SF_6 with a pressure of 50 mTorr , and a plasma created by 50 W of RF power and 300 W of inductive coupling power. Figure 2(E): The etching process creates an undercut, allowing for the deposition of a metallic layer at the bottom of the trench without covering the side walls. A 50 nm layer of aluminum is evaporated to form the gate electrode. Figure 2(F): Lift-off is performed.

Figure 2(G) shows an image of a finished gate at an observation angle of 45° obtained by scanning electron microscopy (SEM). Trenches and gates with a width as small as 200 nm have been successfully obtained with this process.

2.2. Transfer of graphene monolayers above the gate

Graphene monolayers are transferred above the gate using a modified version of the method described in Ref. [38], where cellulose acetate butyrate (CAB) is used as the

transfer medium. To allow for an alignment with a precision of a few micrometers, the critical steps of the transfer are performed with the help of a micromanipulator based on a probe station originally designed for electrical measurements. The micromanipulator features a stage with horizontal and vertical translation control, a microscope, and two needle pins with XYZ control.

The graphene transfer step proceeds as follows. First, after the local gate is fabricated, the substrate (from now referred to as the destination substrate) is covered with PMMA. Next, electron beam lithography is performed to open a window of $100 \times 100 \mu\text{m}^2$ centered on the location where graphene is to be transferred. The PMMA acts as a protective layer as the transfer process would otherwise contaminate the destination substrate with graphite residues.

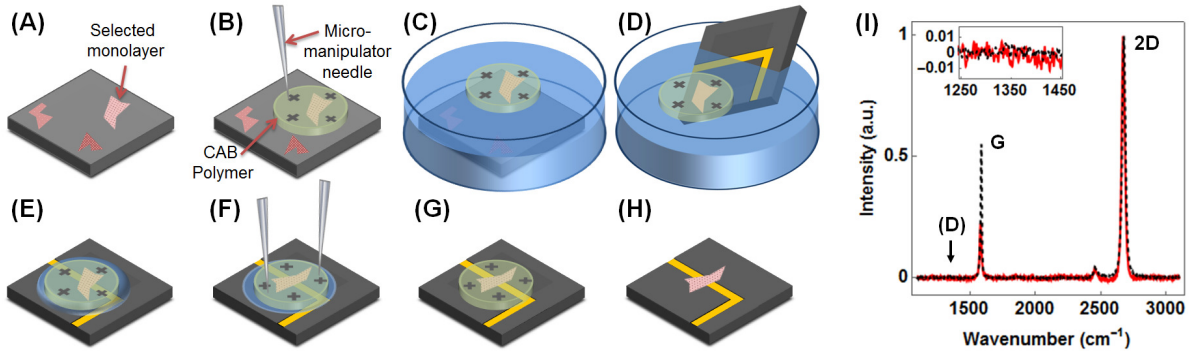


Figure 3. (color online) Graphene monolayer transfer process. (A) Graphene is mechanically exfoliated on a Si/SiO₂ substrate and a monolayer is selected. (B) A drop of CAB polymer covers the selected monolayer. After the polymer is dried markers are patterned using the needles of a micromanipulator. (C) The CAB polymer peels off in deionized water, holding the graphene flake on its bottom side. (D) The CAB polymer is brought on top of the destination substrate. (E) The CAB polymer lies on the destination substrate with a water interface layer. (F) The micromanipulator needles hold the CAB polymer in place whereas the substrate is positioned with the micromanipulator stage. (G) The substrate is baked to evaporate the water film. (H) The CAB polymer and the protecting PMMA resist are dissolved, leaving the transferred monolayer on the destination substrate. (I) Raman spectra of a graphene monolayer before (black dashed line) and after (full red line) transfer. Both spectra were normalized so that the 2D peak maximum intensity is 1 (in arbitrary units). The intensity ratios between the G and 2D peaks are different because of the different substrates [39]. The inset zooms on the region where a D peak would appear if the graphene had been damaged by the transfer.

Graphene layers are then obtained by mechanical exfoliation of kish graphite onto a separate Si/SiO₂ substrate (figure 3(A)), which we call the exfoliation substrate. Using Si/SiO₂ as a substrate enables the discrimination of one to few layer flakes by inspection with an optical microscope [40]. The number of layers is then confirmed by Raman spectrometry [41], and a monolayer is selected for the transfer step to follow. A solution of cellulose acetate butyrate (CAB) in ethyl acetate 60 mg/mL, which is a hydrophobic

polymer, is dripped onto the substrate, covering the graphene monolayer of interest. The latter is still distinguishable under the optical microscope after the CAB polymer dries off. The needles of the micromanipulator are used to punch markers around the monolayer (figure 3(B)). These markers will later allow for the alignment of the graphene relative to the gate on the destination substrate, onto which graphene is optically indiscernible.

Next, the exfoliation substrate is slowly dipped into deionized water (figure 3(C)). Since the SiO_2 substrate is hydrophilic while the CAB polymer is hydrophobic, water peels off the CAB polymer away from the substrate, whereas the graphene remains attached to the bottom of the polymer [38]. The polymer is then laid on top of the destination substrate (figure 3(D)). A film of water with thickness controlled by suction with a pipette separates the polymer from the destination substrate, allowing for the alignment of one relative to the other (figure 3(E)).

The alignment is achieved using the micromanipulator with needles poking into the polymer and holding it at a fixed position, while the substrate, which is attached to the stage, is displaced (figure 3(F)). The alignment is performed with the help of the markers previously defined onto the polymer. The precision of this alignment procedure is approximately 5 microns, which is sufficient given the typical graphene monolayer size. The substrate is then baked at 80°C for about 10 minutes to evaporate the water film (figure 3(G)). After baking, the CAB polymer and the underlying protecting PMMA layer are dissolved in acetone (figure 3(H)). The device is further cleaned in acetone and isopropanol and finally blow-dried with nitrogen gas. In contrast to many fabrication methods of suspended graphene devices [33, 29], our process does not require critical point drying.

The transfer area is next imaged by SEM at low electron dose (less than $1\ \mu\text{C}/\text{cm}^2$ at 10 keV) to prevent damaging the graphene layer [42, 43, 44]. The purpose of this observation is to ensure that the graphene overlaps with the trench continuously, and that large enough areas of graphene are present on both sides of the trench, minimizing the contact resistance with the electrodes to be patterned. Furthermore, precise measurements of the position of the graphene flake are performed to prepare the alignment of the next EBL step (patterning of electrodes).

Finally, Raman spectrometry is performed to check the quality of the graphene monolayer after transfer (figure 3(I)). The absence of D peak in the Raman spectrum ensures that the graphene has not been degraded during the transfer process followed by SEM observation [42, 43, 44].

2.3. Patterning of electrodes

In the last step of the fabrication process, contact electrodes are patterned using EBL. The substrate is coated with a PMMA monolayer. After the resist is exposed and developed, 5 nm of titanium and subsequently 50 to 120 nm of aluminum are evaporated. The final device is obtained after a lift-off step. Again, no critical point drying is required.

Electrodes are designed in such a way that at least a few micron squared of graphene are covered on each side of the trench to minimize contact resistance. Ideally, the metal should slightly overlap the trench close to the edge so that the graphene junction area is fully suspended. For the device with $W = 7 \mu\text{m}$, this has not been possible due to lift-off problems. However, we expect that with further improvements in the fabrication process it will be possible to obtain samples where the graphene flake is fully suspended between the contacts. Graphene junctions of length L (cf. figure 1(B)) designed from 300 to 500 nm were successfully fabricated. With this monolayer resist process, lift-off is difficult on devices with shorter junctions. Due to the long aspect ratio of the junctions ($W \geq 5 \mu\text{m}$) a bilayer process is difficult to implement because the resist bridge defining the junction collapses. After the lift-off, no temperature annealing is performed. The device is ready to be measured.

3. Results and discussion of electrical measurements

In this section, we present and discuss voltage versus current (V-I) characteristics measured on a typical device. On this sample, the trench is 360 nm wide and the graphene-gate separation is 180 nm. The designed dimensions of the junction considered here are $W = 7 \mu\text{m}$ and $L = 500 \text{ nm}$. Other devices have been measured; their properties are summarized at the end of this section. As will be described in this section, the devices are not suitable for room temperature use due to the presence of thermal carriers in the substrate. These carriers open a current leakage channel between the gate and electrodes, which masks the regular field effect behaviour. As our device has the specificity to not include a truly insulating layer to separate the gate from the electrodes and the conducting channel, we provide a simple model to quantitatively estimate the leakage currents. This information will help the interested reader to adapt our process to room temperature applications by choosing a more appropriate substrate. The main part of this section focuses on the mobility in the low-temperature regime, where current leakages are suppressed and regular FET behaviour is recovered.

3.1. V-I characteristics of junctions

To measure the electric properties of the suspended junctions, the device is glued onto a printed circuit board (PCB) and wire-bonded. The PCB is attached and electrically connected to a sample holder. The sample holder is a copper box shielding the device from electromagnetic noise. Each biasing or measurement port is filtered by a two-stage RC low-pass filter (cutoff frequency ranging from 1 kHz to 2 MHz) in series with a copper powder filter to eliminate higher frequency noise. The sample holder is placed in vacuum in a cryostat enabling measurements from room temperature down to 4 K.

Figure 4 shows the measurement setup. The junction is biased with a current I_B delivered by a Yokogawa 7651 source. The voltage drop V_m is measured by an

Agilent 34401A multimeter. The gate voltage V_g is applied between the gate electrode and the ground by another Yokogawa 7651 source used in voltage mode. R_i , R_v and R_g are the series resistance added by the filters in the sample holder for the current, voltage and gate voltage leads, respectively. Since only direct current behaviour is of interest here, capacitors of the RC filters are not shown. At the chip level (area enclosed in the blue dashed line on figure 4) the junction is modeled by a resistor R_J , which is modulated by the gate voltage V_g applied through the capacitor C_g . Unlike the other capacitances, C_g is specifically shown for illustration purposes. The resistors R_L , R'_L model parasitic resistances between the gate and source/drain electrodes, as will be discussed in detail below.

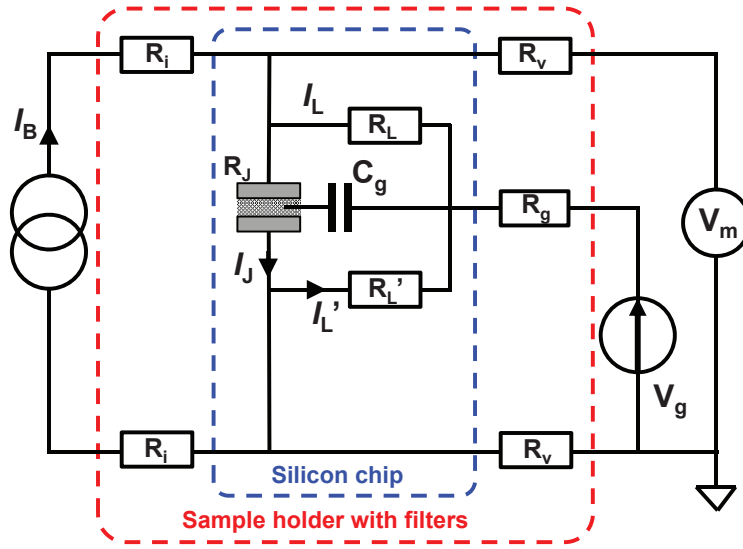


Figure 4. (color online) Electrical circuit modeling the junction in its measurement environment in the presence of gate leakage. The inner dashed (blue) contour encloses the silicon chip space, with parasitic leakage resistances R_L and R'_L . The outer dashed (red) contour represents the sample holder space that includes low-pass filters determined by resistors R_i and R_v and capacitors (not shown).

Figure 5 shows three sets of V-Is with varying gate voltages V_g , corresponding to three different temperatures (300 K, 77 K and 4 K). Symbols are data points, and lines are linear fits.

At room temperature V-Is exhibit a nonconventional behaviour: except for $V_g = 0$ (larger dots), the V-Is display a non-zero voltage at zero bias current: $V_m(I_B = 0) \neq 0$. As it will be explained quantitatively in the next subsection, we attribute this offset to gate leakages, *i.e.* a conduction path between the gate and the electrodes. Indeed, unlike common field-effect devices, in our device there is no truly insulating layer (such as silicon oxide or silicon nitride) between gate and electrodes, since both lie on the same substrate. The resistivity ρ_{Si} of our silicon wafers is chosen to be very high ($\rho_{Si} > 10 \text{ k}\Omega\cdot\text{cm}$) but it is still much smaller than the resistivity of a good insulator (e.g. $\rho_{SiO_2} = 10^{14} - 10^{16} \Omega\cdot\text{cm}$).

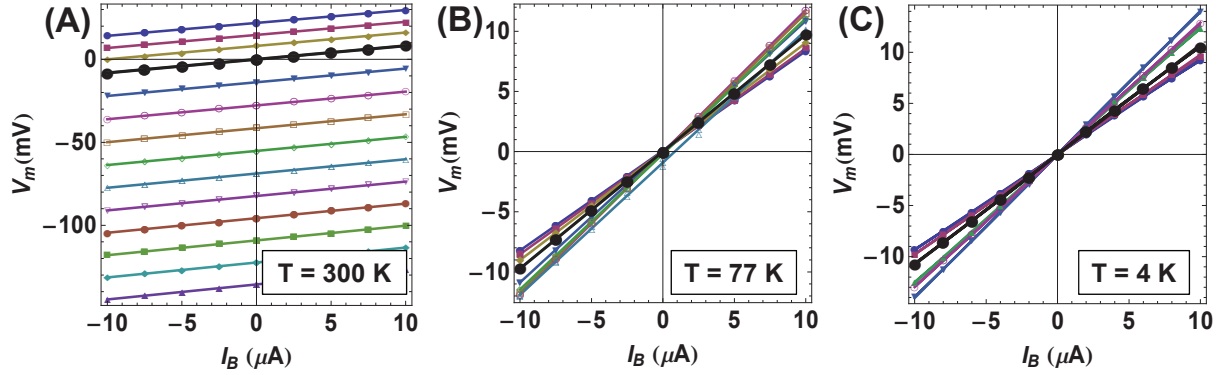


Figure 5. V-I characteristics of the device for various gate voltages V_g and 3 different temperatures. On all the panels the symbols are data points, whereas lines are linear fits. The thicker lines with thicker symbols show $V_m(I)$ at $V_g = 0$. (A) $T = 300$ K. $V_g = -10$ V (bottom) to 3 V (top) in 1 V steps. (B) $T = 77$ K. $V_g = -5$ V to 3 V in 1 V steps. (C) $T = 4$ K. $V_g = -3$ V to 2 V in 1 V steps.

At lower temperatures, the V-Is don't show any offset as long as $|V_g|$ is kept below a threshold value, typically a few volts. When $|V_g|$ is larger than this threshold, the offset kicks in quickly and the V-Is become noisy and non-reproducible. Therefore, we avoid to work in this regime, and the V-Is shown on figures 5.(B) and (C) are confined to a smaller V_g range than figure 5.(A).

To allow for a quantitative analysis of the data, we fit each V-I curve to a straight line $V_m(I_B) = \eta I_B + V_0$. $\eta(V_g)$ is the slope in Ohms and $V_0(V_g)$ is the offset discussed above. Figure 6 shows η and V_0 versus gate voltage V_g for the data sets presented on figure 5. The error bars on V_0 have several origins: the standard deviation of the fitting procedure, the accuracy of the voltmeter and the accuracy of the current source.

In an ideal field-effect device the slope η of the V-I is equal to the V_g -dependent junction resistance R_J . However, because of current leakages through the gate, part of the bias current I_B doesn't flow through the junction. We present in the next subsection a model to take these leakage paths into account.

3.2. Circuit model

To quantitatively understand the V-Is presented in the previous subsection we need to account for gate leakages, *i.e.* the finite currents I_L and I'_L flowing between the gate and the electrodes through the substrate. We model this effect by adding resistors of finite value R_L and R'_L , respectively, between the gate and each electrode (cf. figure 4). In the following we will assume that $R_L = R'_L$ due to the symmetry of the device. Using Kirchhoff laws, we can calculate the dependence of the fitting parameters η and V_0 introduced above

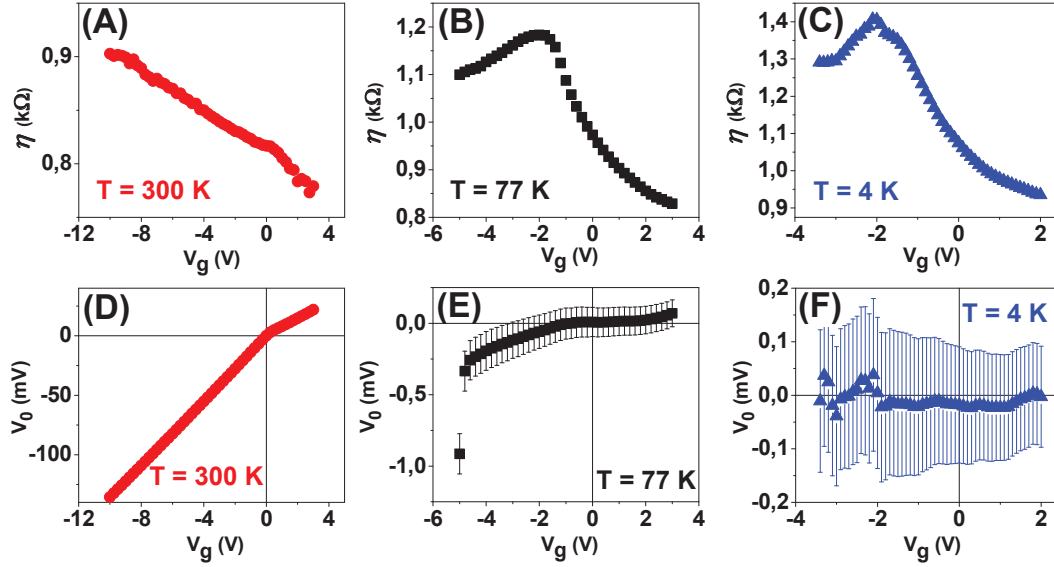


Figure 6. (color online) Fitted slopes η (a-c) and vertical offset V_0 (d-f) of the V-Is shown on figure 5. For panels (A), (B), (C) and (D) the error bars are smaller than the symbols.

on the circuit parameters, and so express the junction R_J and leakage R_L resistances as :

$$R_J \simeq \eta, \quad (1)$$

and

$$R_L \simeq \frac{(2R_v + \eta)V_g - 2R_g V_0}{V_0}. \quad (2)$$

The expressions above are approximations neglecting terms according to $R_v \ll R_g$ and $V_0/V_g \ll 1$. Before investigating in the next subsection the field-effect properties of the device (variations of R_J versus V_g), we discuss the gate leakage determined based on Eq.2.

Extracting R_L from the fitted η and V_0 using Eq.2 involves a division by V_0 . Thus when the uncertainty δV_0 on V_0 is larger than V_0 itself, the inferred value for R_L is meaningless and should be discarded. On figure 6 we see that reliable values of R_L can be extracted only at room temperature and for a few points at 77 K. At 4 K the leakage resistance cannot be reliably extracted for any value of the presented gate voltage range; however we have also measured V-Is at larger V_g (data not shown) so that R_L can be estimated.

At room temperature R_L is nearly constant for $V_g < 0$ with a value of 2 M Ω which increases to 7 M Ω as V_g is increased from zero to 2 V. We considered a model for the leakage resistance based on two back-to-back Schottky diodes due to the two metal-semiconductor interfaces, and a resistor describing conduction through the silicon substrate. This model leads to a nearly V_g -independent resistance of 3 M Ω for $V_g < 0$, and larger values for

$V_g > 0$, reaching up to $32 \text{ M}\Omega$ for $V_g = 2 \text{ V}$. The agreement is satisfactory given the simplicity of the model and is a strong indication that Schottky barriers and conduction through the substrate are the sources of the measured resistance.

At 77 K and 4 K the leakage resistance is enhanced by at least two orders of magnitude: $R_L \approx 1$ to $2 \text{ G}\Omega$ in the V_g range where it is computable. In the V_g range where R_L is not computable, we note that $|V_0|$ tends to be smaller than outside this range. In our parameter range, Eq.2 is dominated by a term proportional to $1/V_0$ so the value of R_L computed for V_g at the border of the domain of the validity is a lower bound of the actual R_L in the inaccessible range. We can then conclude that for $V_g \approx 0$, $R_L \geq 2 \text{ G}\Omega$ both at 77 K and 4 K . This is consistent with an enhancement of the resistivity of the substrate (intrinsic silicon) and of the Schottky junctions as the temperature is lowered.

In conclusion, gate leakage plays a significant role at room temperature, offsetting the V-Is vertically for arbitrarily small values of the gate voltage V_g and disturbing the FET behaviour. However at low temperature ($T \leq 77 \text{ K}$) gate leakage is strongly suppressed and is negligible over a fairly large range of V_g . We expect that using as a substrate a higher gap insulator than silicon, for example sapphire, will lead to effective suppression of leakage at room temperature.

3.3. Field-effect

Now we analyze the measured $R_J(V_g)$ at low temperature (77 K and 4 K) in terms of field effect. The mobility μ of the carriers in the graphene junction is given by:

$$\mu = \frac{1}{\rho_s e n_{\text{tot}}}, \quad (3)$$

where $\rho_s = R_J W/L$ is the sheet resistivity of the graphene channel with R_J extracted from data using Eq. 1, $-e$ is the electron charge and n_{tot} is the carrier surface density. $n_{\text{tot}} = n_g + n_b$ is the sum of two contributions: n_g , induced by the gate electric field, and a background n_b due to thermally excited carriers as well as charges trapped in the vicinity of the graphene sheet. Using a parallel plate capacitor model,

$$n_g = \frac{\epsilon_0 \epsilon_r}{t e} V_g, \quad (4)$$

where ϵ_0 is the vacuum permittivity, $\epsilon_r = 1$ is the relative permittivity of the insulator (here vacuum) and $t = 180 \text{ nm}$ is the separation between the gate surface and the graphene sheet. We note that for carrier densities up to $n = 2 \times 10^{11} \text{ cm}^{-2}$ the attractive electrostatic force between the gate and the graphene bridge does not exceed 11 nN [33], yielding a maximum deflection of 2 nm [45]. Thus we can neglect the dependence of t on the gate voltage in the range explored in the experiment.

The other contribution, n_b , to the carrier surface density is constant and determined by setting the condition $n_{\text{tot}}(V_g = V_{\text{CNP}}) = 0$. V_{CNP} is the charge neutrality point, *i.e.* the gate voltage for which $R_J(V_g)$ reaches a maximum, determined experimentally (cf. figure 7(A)). Ideally at V_{CNP} the Fermi level in graphene is set exactly at the point where

conduction and valence bands meet, yielding theoretically a zero density of carriers and an infinite resistance. However in practice local fluctuations prevent from nulling exactly the density of carriers [46], and a finite maximum of resistance is observed. In that region n_{tot} becomes independent of V_g and Eq. 3 is not valid. Defining $n_{\text{sat}} = 2 \cdot 10^{11} \text{ cm}^{-2}$ as the total carrier density below which $R_J(n_{\text{tot}})$ saturates [15], the mobility μ can be evaluated for $|n| > n_{\text{sat}}$ as:

$$\mu = \frac{t}{\epsilon_0 \epsilon_r \rho_s (V_g - V_{\text{CNP}})}. \quad (5)$$

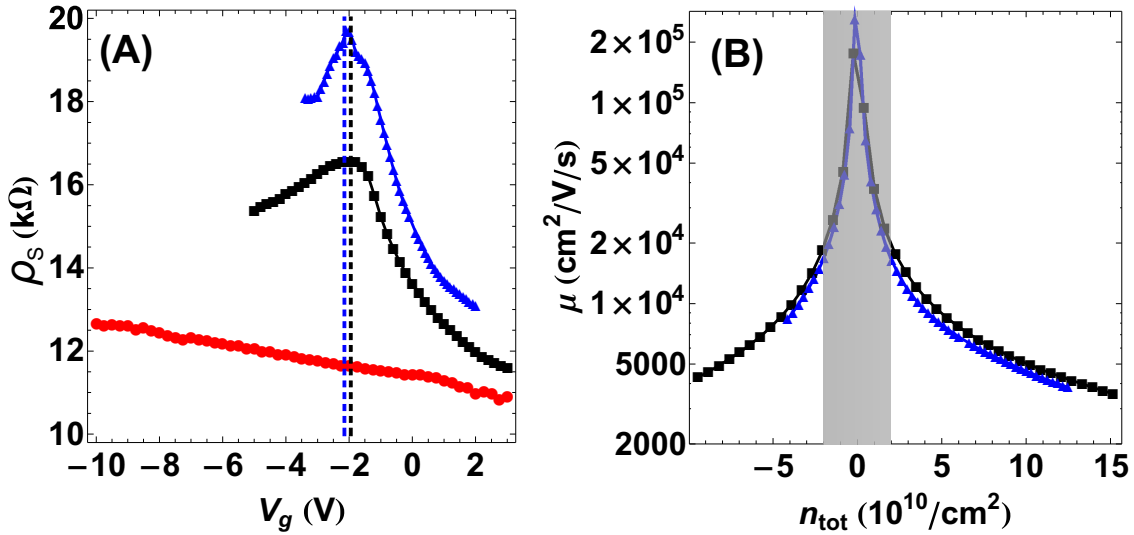


Figure 7. (color online) (A): Sheet resistivity ρ_s and (B) mobility μ extracted from data presented in figure 5, at 300 K (red dots), 77 K (black squares) and 4 K (blue triangles). On panel (A) the vertical lines show the position of the charge neutrality point at 77 K (dashed black lines) and 4 K (dotted blue line). On panel (B) the shaded area masks the domain where Eqs. 3 and 5 do not hold, resulting in an artificial boost of the mobility.

Figure 7 shows the sheet resistivity ρ_s and the mobility μ for the junction presented earlier. Although the resistivity increases with decreasing temperature, the mobility is rather temperature insensitive. At $n = 10^{11} \text{ cm}^{-2}$, $\mu \approx 5100 \text{ cm}^2/\text{V/s}$, which is typical for graphene FETs. In non-suspended [47, 32] and suspended [33, 29] graphene junctions however, it has been reported that current annealing can improve the mobility by an order of magnitude. We applied this approach to our junctions. Up to a current density of $1.5 \text{ mA}/\mu\text{m}$, we indeed observed an increase in mobility, but only marginally (by less than a factor of 2). Above $1.5 \text{ mA}/\mu\text{m}$, further annealing has no effect or degrades the mobility. Above $3 \text{ mA}/\mu\text{m}$, all the tested junctions were damaged. A systematic effect of current annealing though is the reduction of V_{CNP} , bringing it closer to zero gate voltage in agreement with the fact that current annealing cleans the device from charges trapped in the vicinity of the junction [47, 48].

Device	W (μm)	L (nm)	$\rho_{\text{CNP}}^{300\text{K}}$ ($\text{k}\Omega$)	$\rho_{\text{CNP}}^{77\text{K}}$ ($\text{k}\Omega$)	$\rho_{\text{CNP}}^{4\text{K}}$ ($\text{k}\Omega$)	$\mu^{77\text{K}}$ at $n = 10^{11} \text{ cm}^{-2}$ ($\text{cm}^2/\text{V/s}$)
W67-8-3	7	500	NA	16.5	19.7	5100
W67-8-2	5	500	NA	10.5	10.2	11500
W67-6-1	4	350	14.5	14.0	NA	2010

Table 1. Summary of results on measured devices. ρ_{CNP} is the maximum sheet resistivity at the charge neutrality point when it is accessible. μ is given at 77 K. NA stands for "not available".

Table 1 sums up the values of resistivity and mobility measured on three devices. The sheet resistivity at the charge neutrality point ρ_{CNP} at 4 K is given before current annealing. The latter was found to slightly change ρ_{CNP} (up to +17% and down to -7%), without sizeable effect on the mobility. The mobilities are given at 77 K, but data at 4 K, when available, show that the mobility drops by $\approx 10\%$ compared to the 77 K value.

The graphene junctions presented in this work have a sheet resistance and a mobility similar to those of state-of-the-art graphene FETs, although their mobility is comparable only to unsuspended devices. However this is sufficient to fabricate graphene-based Josephson junctions [32, 49].

Before concluding, we note that related processes to transfer and suspend graphene on top of existing structures were recently published [30, 31]: in those works the transfer medium is either a PDMS or PMMA film and the electrical contact to the rest of the circuit is performed by stamping this film directly onto metallic electrodes. While these methods may be successful to build graphene FETs, no DC electrical characterization is presented although very promising results were obtained at RF-frequencies [31, 23]. Patterning contacts by metal evaporation on top of a graphene layer, as done in our process, is a well established and reliable method to obtain low resistance ohmic contacts required for DC applications, and it allows for a precise definition of the geometry of the contacts.

Conclusions

We presented a fabrication method for field-effect transistors made of a graphene monolayer sheet suspended above a local metallic gate and lying on an insulating substrate. In these first experiments, the sheet resistivities and mobilities of the devices at low temperature are comparable to those of unsuspended graphene devices. The devices described in this work constitute a viable route towards graphene-based superconducting quantum devices. First, the measured mobilities are expected to be sufficient to build graphene Josephson junctions with critical current tunable by the gate voltage. Second, in contrast with graphene devices gated by a doped substrate, using an insulating substrate provides an environment compatible with superconducting qubits and circuit-

QED experiments. Indeed, energy loss through the radiofrequency excitation of substrate carriers is suppressed, increasing the coherence time of quantum devices. Finally, local gating enables the independent control of individual graphene junctions on the same chip, which is decisive for scalability. The fabrication process we describe in this paper is also of interest for investigations of the nano-electromechanical properties of graphene. We finally note that the transfer and suspension method could be applied to fabricate devices incorporating 2D materials other than graphene, including boron nitride or molybdenum disulfide.

Acknowledgements

We thank Thomas Szkopek and Elisabeth Ledwosinska for useful discussions, and Martin Otto for help with the experiments. We thank the Nanofab team at IQC, in particular Nathan Nelson-Fitzpatrick, for their advice all along the development of the fabrication process. We are grateful to Liyan Zhao and the Waterloo Advanced Technology Lab for their help with the Raman spectrometer. We thank Pol Forn-Diaz for valuable inputs to the manuscript. This work was supported by the Natural Sciences and Engineering Research Council of Canada, the Canada Foundation for Innovation, the Ontario Ministry of Research and Innovation, and CMC Microsystems. During this work, Adrian Lupascu was supported by an Alfred Sloan Foundation Fellowship.

References

- [1] Novoselov K S, Geim A K, Morozov S, Jiang D, Zhang Y, Dubonos S, Grigorieva I and Firsov A 2004 *Science* **306** 666
- [2] Novoselov K, Geim A K, Morozov S, Jiang D, Katsnelson M, Grigorieva I, Dubonos S and Firsov A 2005 *Nature* **438** 197
- [3] Zhang Y, Tan Y W, Stormer H L and Kim P 2005 *Nature* **438** 201
- [4] Stander N, Huard B and Goldhaber-Gordon D 2009 *Physical Review Letters* **102** 026807
- [5] Peres N M R, Castro Neto A H and Guinea F 2006 *Physical Review B* **73**(19) 195411
- [6] Miao F, Wijeratne S, Zhang Y, Coskun U, Bao W and Lau C 2007 *Science* **317** 1530
- [7] Heersche H B, Jarillo-Herrero P, Oostinga J B, Vandersypen L M and Morpurgo A F 2007 *Nature* **446** 56
- [8] Berger C, Song Z, Li T, Li X, Ogbazghi A Y, Feng R, Dai Z, Marchenkov A N, Conrad E H, First P N *et al.* 2004 *The Journal of Physical Chemistry B* **108** 19912
- [9] Geim A K and Novoselov K S 2007 *Nature Materials* **6** 183
- [10] Schwierz F 2010 *Nature Nanotechnology* **5** 487
- [11] Weiss N O, Zhou H, Liao L, Liu Y, Jiang S, Huang Y and Duan X 2012 *Advanced Materials* **24** 5782
- [12] Poot M and van der Zant H S 2012 *Physics Reports* **511** 273
- [13] Chen C and Hone J 2013 *Proceedings of the IEEE* **101** 1766
- [14] Sabio J, Seoanez C, Fratini S, Guinea F, Neto A C and Sols F 2008 *Physical Review B* **77** 195409
- [15] Du X, Skachko I, Barker A and Andrei E Y 2008 *Nature Nanotechnology* **3** 491
- [16] Dean C, Young A, Meric I, Lee C, Wang L, Sorgenfrei S, Watanabe K, Taniguchi T, Kim P, Shepard K *et al.* 2010 *Nature nanotechnology* **5** 722

- [17] Tan Y W, Zhang Y, Stormer H L and Kim P 2007 *The European Physical Journal Special Topics* **148** 15
- [18] Jeong D, Choi J H, Lee G H, Jo S, Doh Y J and Lee H J 2011 *Physical Review B* **83** 094503
- [19] Titov M and Beenakker C W 2006 *Physical Review B* **74** 041401
- [20] Dubos P, Courtois H, Pannetier B, Wilhelm F, Zaikin A and Schön G 2001 *Physical Review B* **63** 064502
- [21] Lee G H, Jeong D, Choi J H, Doh Y J and Lee H J 2011 *Physical Review Letters* **107** 146605
- [22] Girit C, Bouchiat V, Naaman O, Zhang Y, Crommie M, Zettl A and Siddiqi I 2008 *Nano Letters* **9** 198
- [23] Singh V, Bosman S, Schneider B, Blanter Y, Castellanos-Gomez A and Steele G 2014 *Nature Nanotechnology* **9** 820
- [24] Martinis J M, Cooper K, McDermott R, Steffen M, Ansmann M, Osborn K, Cicak K, Oh S, Pappas D, Simmonds R *et al.* 2005 *Physical Review Letters* **95** 210503
- [25] Megrant A, Neill C, Barends R, Chiaro B, Chen Y, Feigl L, Kelly J, Lucero E, Mariantoni M, OMalley P *et al.* 2012 *Applied Physics Letters* **100** 113510
- [26] Orgiazzi J L, Deng C, Layden D, Marchildon R, Kitapli F, Shen F, Bal M, Ong F and Lupascu A 2014 *arXiv preprint arXiv:1407.1346*
- [27] Liao L, Bai J, Qu Y, Lin Y c, Li Y, Huang Y and Duan X 2010 *Proceedings of the National Academy of Sciences* **107** 6711
- [28] Grushina A L, Ki D K and Morpurgo A F 2013 *Applied Physics Letters* **102** 223102
- [29] Lau C N, Bao W and Velasco Jr J 2012 *Materials Today* **15** 238
- [30] Castellanos-Gomez A, Buscema M, Molenaar R, Singh V, Janssen L, van der Zant H S and Steele G A 2014 *2D Materials* **1** 011002
- [31] Weber P, Guttinger J, Tsioutsios I, Chang D and Bachtold A 2014 *Nano Letters* **14** 2854
- [32] Ojeda-Aristizabal C, Ferrier M, Guéron S and Bouchiat H 2009 *Physical Review B* **79** 165436
- [33] Bolotin K I, Sikes K, Jiang Z, Klima M, Fudenberg G, Hone J, Kim P and Stormer H 2008 *Solid State Communications* **146** 351
- [34] Mizuno N, Nielsen B and Du X 2013 *Nature Communications* **4** 2716
- [35] Zhang Y, Mendez E E and Du X 2011 *ACS Nano* **5** 8124
- [36] Balandin A A 2013 *Nature Nanotechnology* **8** 549
- [37] Bunch J S, Van Der Zande A M, Verbridge S S, Frank I W, Tanenbaum D M, Parpia J M, Craighead H G and McEuen P L 2007 *Science* **315** 490
- [38] Schneider G F, Calado V E, Zandbergen H, Vandersypen L M and Dekker C 2010 *Nano Letters* **10** 1912
- [39] Wang Y Y, Ni Z H, Yu T, Shen Z X, Wang H M, Wu Y H, Chen W and Shen Wee A T 2008 *The Journal of Physical Chemistry C* **112** 10637
- [40] Blake P, Hill E, Castro Neto A, Novoselov K, Jiang D, Yang R, Booth T and Geim A 2007 *Applied Physics Letters* **91** 063124
- [41] Ferrari A, Meyer J, Scardaci V, Casiraghi C, Lazzeri M, Mauri F, Piscanec S, Jiang D, Novoselov K, Roth S *et al.* 2006 *Physical Review Letters* **97** 187401
- [42] Teweldebrhan D and Balandin A A 2009 *Applied Physics Letters* **94** 013101
- [43] Murakami K, Kadowaki T and Fujita J i 2013 *Applied Physics Letters* **102** 043111
- [44] Childres I, Jauregui L A, Foxe M, Tian J, Jalilian R, Jovanovic I and Chen Y P 2010 *Applied Physics Letters* **97** 173109
- [45] Fogler M, Guinea F and Katsnelson M 2008 *Physical Review Letters* **101** 226804
- [46] Martin J, Akerman N, Ulbricht G, Lohmann T, Smet J, Von Klitzing K and Yacoby A 2008 *Nature Physics* **4** 144–148
- [47] Moser J, Barreiro A and Bachtold A 2007 *Applied Physics Letters* **91** 163513
- [48] Cheng Z, Zhou Q, Wang C, Li Q, Wang C and Fang Y 2011 *Nano Letters* **11** 767
- [49] Du X, Skachko I and Andrei E Y 2008 *Physical Review B* **77** 184507